#AP2

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. MCT.0102US

In Re Application Of: **Paul Petersen**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/419,523	10/18/1999	Christian Chase	21906	2189	1377

Invention: **Determining Memory Upgrade Options**

COMMISSIONER FOR PATENTS:

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August 30, 2006

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Dated: **November 6, 2006**

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Applicant:	Paul Petersen	§	Group Art Unit:	2187
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Janice Munoz

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REAL PARTY IN INTEREST

The real party in interest is the assignee Micron Technology.

RELATED APPEALS AND INTERFERENCES

This application was previously appealed, in Appeal No. 2004-0037, which resulted in a Decision on Appeal being mailed out on August 31, 2004.

STATUS OF CLAIMS

The application was originally filed with claims 1-20. Claims 21-40 were subsequently added during prosecution of the application and were the subject of Appeal No. 2004-0037. After the Decision on Appeal that was mailed out on August 31, 2004, claims 1-40 were cancelled and claims 41-68 were added. Claims 52, 61, 66 and 68 have been subsequently cancelled, leaving claims 41-51, 53-60, 62-65 and 67, which have been finally rejected and are the subject of the present appeal.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

Regarding independent claim 41, claim 41 recites a method that includes obtaining memory configuration information of a computer system. In a particular embodiment, the specification describes a memory configuration routine 112 that obtains memory configuration information. Specification, ll. 20-23, p. 2. The method of claim 41 also includes determining a memory capacity of a computer system, including executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system. The specification describes execution of the memory configuration routine 112 to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system. Specification, ll. 15-21, p. 5. The method of claim 41 also includes automatically determining memory upgrade options based on the determined memory capacity of the computer system. The specification describes the memory configuration routine 112 as determining memory upgrade options based on determined memory capacity. Specification, ll. 3-17, p. 6.

Regarding independent claim 54, the specification describes a program storage device 113 that stores executable code for the memory configuration routine 112. Specification, ll. 24-25, p. 4. The instructions when executed cause a programmable control device to obtain memory configuration information of a computer system, as set forth in the specification's description of the memory configuration routine 112. Specification, ll. 20-23, p. 2. The memory configuration routine 112 also determines a memory capacity for the computer system, including determining a maximum number of device sockets that can be supported by a memory controller of the computer system. Specification, ll. 15-21, p. 5. Additionally, the memory configuration routine 112 determines memory upgrade options based on the determined memory capacity of the computer system. Specification, ll. 3-17, p. 6.

Regarding independent claim 62, the specification discloses a computer system 100. *See, for example*, Fig. 1 and the general description of system 100 in lines 20-30 of page 2 and lines 1-28 on page 3 of the specification. The specification describes a processor 102 of the computer system 100. Specification, ll. 3-4, p. 3. The specification also describes a system memory that is

coupled to the processor. The system memory has one or more memory modules and a memory configuration. The memory modules include one or more memory devices. Specification, ll. 1-4, p. 4. The specification also describes a memory configuration routine 112 that includes instructions to obtain memory configuration information, determine a memory capacity of the computer system, including determining a maximum number of memory devices that can be supported per memory bus channel of the computer system and determine memory upgrade options based on the determined memory capacity. Specification, ll. 15-21, p. 5 and ll. 3-17, p. 6.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. **Do Claims 41-51, 53-60, 62-65 and 67 Fail to Comply with the Enablement Requirement of 35 U.S.C. § 112, First Paragraph?**

B. **Do Claims 41-51, 53-60, 62-65 and 67 Fail to Comply with the Written Description Requirement of 35 U.S.C. § 112, First Paragraph?**

C. **Are Claims 41, 42, 45, 48, 49, 51, 53-55, 58-60, 62-65 and 67 Rendered Obvious in view of Arai (U.S. Patent No. 5,280,599) and Yoshizawa (U.S. Patent No. 5,787,464)?**

ARGUMENT

A. Do Claims 41-51, 53-60, 62-65 and 67 Fail to Comply with the Enablement Requirement of 35 U.S.C. § 112, First Paragraph?

The Examiner contends that claims 41-51, 53-60, 62-65 and 67 fail to comply with the enablement requirement due to the purported failure of the specification to describe either how a software routine determines a maximum number of memory devices that can be supported through a memory bus channel of a computer system (claims 41-51, 53, 62-65 and 67) or how instructions when executed cause a programmable control device to determine a maximum number of memory sockets that can be supported by a memory controller (claims 54-60). The contested language appears in independent claims 41, 54 and 62.

The specification, at least on page 5, provides support and an enabling disclosure for the determination language of claims 41, 54 and 62. More particularly, on page 5, the specification discusses that the memory configuration routine 112 determines a total memory capacity for the computer system 100. The specification states that this function may either be performed by BIOS routines or alternatively, may be retrieved from a non-volatile storage device 114. Specification, ll. 15-21, p. 5. The specification also describes that in determining memory capacity, the routine 112 may account for the maximum number of memory sockets for the memory controller. Specification, ll. 22-30, p. 5.

Thus, the specification clearly enables one skilled in the art to build a system that executes a routine that determines a maximum number of memory devices that can be supported through a memory bus channel of a computer system and determines the maximum number of memory sockets that a memory controller supports. According to the embodiments that are described in the specification, one such technique may be, for example, the prior knowledge that there is a limit of 32 devices per memory channel, and this information may be stored in a non-volatile storage device. Thus, the specification clearly describes that the memory routine 112 may read this information from the non-volatile storage device 114, a technique which is readily understood by one of ordinary skill in the art. For similar reasons, the specification clearly describes at least one embodiment to determine a memory capacity including determining a maximum number of device sockets that can be supported by a memory controller.

Thus, Applicant submits that the Examiner has not established a *prima facie* case of lack of enablement for claims 41, 54 and 62 or the claims that depend therefrom. As such, the § 112, first paragraph rejection of claims 41-51, 53-60, 62-65 and 67 are in error and should be reversed.

B. Do Claims 41-51, 53-60, 62-65 and 67 Fail to Comply with the Written Description Requirement of 35 U.S.C. § 112, First Paragraph?

Claims 41-51, 53-60, 62-65 and 67 are rejected under 35 U.S.C. § 112, first paragraph. The Examiner contends that the specification fails to set forth a written description for these claims.

However, as set forth above in the discussion of Argument A, the specification clearly sets forth an embodiment in which the memory configuration routine 112, i.e., an executable routine, determines a maximum number of memory devices and can be supported per memory bus channel of a computer system and determines a maximum number of sockets for a memory controller. *See, for example*, lines 15-21 on page 5 of the specification. With this disclosure clearly set forth in the specification, the Examiner has failed to establish a *prima facie* case of lack of written description for claims 41-51, 53-60, 62-65 and 67. Therefore, for at least this reason, Applicant submits that the § 112, first paragraph rejections of claims 41-51, 53-60, 62-65 and 67 based on the alleged lack of a written description is in error and should be reversed.

C. Are Claims 41, 42, 45, 48, 49, 51, 53-55, 58-60, 62-65 and 67 Rendered Obvious in view of Arai (U.S. Patent No. 5,280,599) and Yoshizawa (U.S. Patent No. 5,787,464)?

Claims 41-51, 53-60, 62-65 and 67 stand rejected under 35 U.S.C. § 103(a) in view of the combination of Arai (U.S. Patent No. 5,280,599) and Yoshizawa (U.S. Patent No. 5,787,464). Arai is generally directed to setting expanded and extended memory configurations. In this regard, Arai describes a particular type of memory addressing, called an "expanded memory configuration," which is generally described in lines 22-62 in column 1 of Arai. Arai describes another type of memory addressing, called an "extended memory configuration," which is generally described in lines 63-68 of column 1 and in lines 1-9 of column 2 of Arai. Yoshizawa is generally directed to a system in which memory devices can be added without shutting off the computer system.

A *prima facie* case of obviousness has not been established for any of the § 103 rejections for at least the reason that the hypothetical combination of Arai and Yoshizawa fails to teach or suggest a routine that determines a maximum number of memory devices that can be supported per memory bus channel (claims 41-51, 53, 62-65 and 67) or maximum number of memory sockets for a memory controller (claims 54-60) and automatically determine memory upgrade options based on the determined memory capacity.

More specifically, in the § 103 rejections, the Examiner relies on the RAMBUS data sheet to fill in limitations in the hypothetical combination of Arai and Yoshizawa by way of inherency. However, even assuming, for purposes of argument, that the features disclosed in the RAMBUS data sheet are inherent, a *prima facie* case of obviousness has still not been established for at least the reason that the hypothetical combination fails to teach or suggest all claim limitations.

More specifically, on page 40, the RAMBUS data sheet describes configuration options of a RAMBUS device that may be read from memory. Even assuming, for purposes of argument, that the configuration options disclosed in the RAMBUS data sheet are inherent in Arai, page 40 of the RAMBUS data sheet fails to disclose any configuration information regarding the maximum number of devices per memory bus channel or maximum number of memory sockets for a controller. Thus, although the designer of Arai's computer system may have known of these maximum numbers when the computer system was designed, there is no teaching or suggestion in implementing the determination of these maximum numbers in software or in a software routine. There is no reason why Arai's system or a processor of this system would execute such software during operation to derive this information. Therefore, even assuming that the features that are in the RAMBUS data sheet and referenced by the Examiner are inherent in Arai, there is still no teaching or suggestion for executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel and automatically determine memory upgrade options based on the determined memory capacity.

Likewise, the RAMBUS data sheet also fails to teach or suggest any configuration that indicates the maximum number of device sockets that can be supported by the memory controller. Therefore, even assuming that the limitations of the RAMBUS data sheet are incorporated in Arai, there is no teaching or suggestion in Arai or Yoshizawa regarding

executing software to make this determination for purposes of determining memory upgrade options. Without this showing, a *prima facie* case of obviousness has not bee established for independent claim 54.

Therefore, for at least the reasons that are set forth above, Applicant maintains that the § 103 rejections of claims 41-51, 53-60, 62-65 and 67 are in error and should be reversed.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: November 6, 2006

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CLAIMS APPENDIX

The claims on appeal are:

41. A method to provide memory upgrade information comprising:

obtaining memory configuration information of a computer system;

determining a memory capacity of the computer system, including executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system; and

automatically determining memory upgrade options based on the determined memory capacity of the computer system.

42. The method of claim 41, wherein the act of obtaining memory configuration information comprises obtaining an indication of an installed system memory amount.

43. The method of claim 42, wherein the memory configuration information further comprises a number of memory module sockets.

44. The method of claim 42, wherein the memory configuration information further comprises an operating speed of the installed system memory.

45. The method of claim 41, wherein the act of obtaining memory configuration information comprises accessing a non-volatile storage device.

46. The method of claim 45, wherein the act of accessing a non-volatile storage device comprises accessing a serial presence detect device.

47. The method of claim 41, wherein the act of obtaining memory configuration information comprises obtaining information from one or more dynamic random access memory devices.

48. The method of claim 41, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum number of memory devices for the computer system.

49. The method of claim 41, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum amount of memory for the computer system.

50. The method of claim 41, wherein the act of determining a memory capacity comprises obtaining an indication of a maximum number of memory module sockets for the computer system.

51. The method of claim 41, further comprising providing memory upgrade options to a user.

53. The method of claim 41, wherein the characteristic comprises a limit on the number of memory devices that can be used with a memory controller.

54. A program storage device, readable by a programmable control device, comprising instructions for causing the programmable control device to:

obtain memory configuration information of a computer system;

determine a memory capacity for the computer system, including determining a maximum number of device sockets that can be supported by a memory controller of the computer system; and

determine memory upgrade options based on the determined memory capacity of the computer system.

55. The program storage device of claim 54, wherein the instructions to obtain memory configuration information comprise instructions to obtain an indication of an installed system memory amount.

56. The program storage device of claim 55, wherein the memory configuration information further comprises a number of memory module sockets.

57. The program storage device of claim 54, wherein the instructions to obtain memory configuration information further comprise instructions to obtain an indication of a number of memory module slots available to the programmable control device.

58. The program storage device of claim 54, wherein the instructions to obtain memory configuration information comprises instructions to access a non-volatile storage device.

59. The program storage device of claim 54, wherein instructions to determine a memory capacity comprise instructions to obtain an indication of a maximum number of memory devices for the computer system.

60. The program storage device of claim 54, wherein the characteristic comprises a limit on the number of memory devices that can be installed on a memory channel regardless of the number of open memory slots.

62. A computer system comprising:

a processor;

system memory coupled to the processor, the system memory having one or more memory modules and a memory configuration, wherein the memory modules include one or more memory devices; and

a configuration routine including instructions to obtain memory configuration information, determine a memory capacity of the computer system, including determining a maximum number of memory devices that can be supported per memory bus channel of the computer system of the computer system and determine memory upgrade options based on the determined memory capacity.

63. The computer system of claim 62, wherein the instructions to obtain memory configuration information comprise instructions to obtain indications of installed memory devices.

64. The computer system of claim 62, wherein the instructions to determine a memory capacity comprise instructions to obtain an indication of a maximum amount of memory for the computer system.

65. The computer system device of claim 62, wherein the instructions to obtain memory configuration information comprise instructions to obtain an indication of an installed system memory amount.

67. The computer system of claim 62, wherein the characteristic comprises a limit on the number of memory devices that can be installed on a memory channel regardless of the number of open memory slots.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.